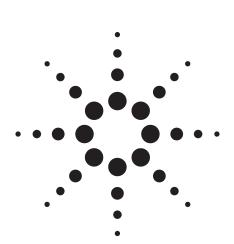
Agilent E4899A 100 Gb/s BERT

PRELIMINARY

Data Sheet Version 0.9



Key Benefits

- Unique data range from 40 Gb/s to 100 Gb/s
- Flexible patterns for stimulus (PRBS and memory based)
- BER (Bit Error Ratio) measurements on ultra-high speed bit patterns
- Standard and proven, turn-key solution
- Electrical differential interfaces with 1.85 mm connectors
- Controlled from user software running on an external Windows XP PC





Enabling future 100 Gb/s Transmission

The new 100 Gb/s Bit Error Ratio Tester (BERT) enables researchers and technologists in universities and research centers to validate their transceiver designs that operate at speeds between 40 and 100 Gb/s.

Based on Proven ParBERT Technology

The E4899A is based on the proven and established ParBERT 81250 hardware and software technology. The parallel signals are supplied by N4872A generators to the multiplexer part of the front-end E4898A.

On the analysis side the input signal is sampled at 1/8 of the data rate and delivered for BER measurement to a N4873A analyzer. To provide ease of use to the operator, a new user interface has been developed which integrates the control of the ParBERT modules. The software user interface has one standard and one password protected expert screen for maintenance purposes.

PRBS and Memory Pattern Generation

The E4899A can generate and analyze standard PRBS polynomials and different memory patterns. Signals can be delivered through differential outputs with single ended signal amplitude from 200 mVpp to 400 mVpp. The analyzer can deal with differential signals within a voltage window of 0 to -800 mV on each input.

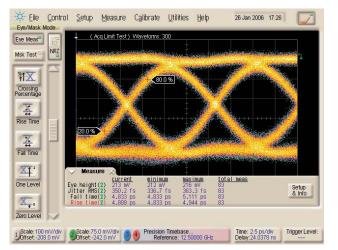


Figure 2: Generator eye diagram at 100 Gb/s

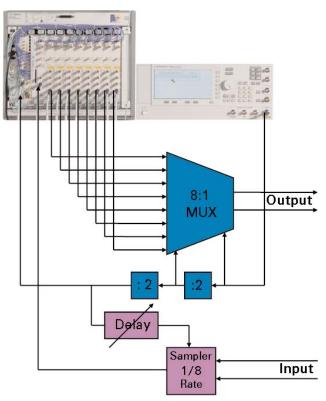


Figure 3: Principle block diagram

| E4898A |
|---|
| File BER System Config |
| BitRate 100,0 Output 400,0 Thres 000.0 [GB/s] 100,0 [mV] 400,0 [mV] 000.0 |
| BER-Measurement |
| Stop Sync CMD 0 CMD 1 BER-Limit 1e-10 |
| Treset Received Bits Wrong Bits BitErrorRate |
| Last 1,25E+10 0 0,00E+00 |
| Total 4,89E+13 0 0,00E+00 |
| Delayline 3 Step (1-100) |
| ParBERT F _{EXT} 12.499999GHz F _{PLL} 12.5GHz |
| Frequency Synthesizer F _{OUT} 50,0 GHz -00.0 dBm RF 0n Supply Service Show Log |



System Specifications

Pattern Generator

Electrical specifications

An electrical differential output is provided on the front-panel of the E4898A.

| Data Rate | 40 Gb/s to 100 Gb/s | |
|------------------------|------------------------------|--|
| Jitter | 400 fs rms | |
| Transition time | 5.5 ps (20/80%) | |
| Data Output | Differential | |
| Connector Type | 50 Ω, 1.85 mm | |
| Single Ended | | |
| Amplitude Range (pp) | 200 to 400 mVpp | |
| Coupling | DC coupled | |
| Logical Levels | V _H 0 - 50 mV | |
| depending on amplitude | $\rm V_L$ -200 mV to -450 mV | |

Patterns

The following patterns are supported: **PRBS:** 2^{7} -1, 2^{9} -1, 2^{10} -1, 2^{11} -1, 2^{15} -1, 2^{23} -1, 2^{31} -1

64 MB of memory on each of the 8 generator channels

Error Detector

An electrical differential input is provided on the front-panel of the E4898A.

The data rate of the error detector is the same as the generator data rate as they are operated by the same clock.

| Data Rate | 40 Gb/s to 100 Gb/s | |
|----------------------|----------------------------|--|
| Data Input | Differential | |
| Connector Type | 50 Ω, 1.85 mm | |
| Receiver Sensitivity | Tbd | |
| Coupling | DC coupled | |
| Input voltage window | 0 to -800 mV on each input | |
| | | |

Patterns

The following patterns are supported: **PRBS:** 2^{7} -1, 2^{9} -1, 2^{10} -1, 2^{11} -1, 2^{15} -1, 2^{23} -1, 2^{31} -1

64 MB of memory on the one analyzer channel

User Interface

The user interface provides access to the following settings:

- Data rate (same for generator and analyzer)
- Generator output levels
- Analyzer sampling delay

The user interface displays the measured Bit Error Ratio (BER). It also provides access to maintenance functions to be used by trained personnel.

Operating System

The software supplied runs on Windows 2000 and Windows XP.

General

| Power supply | 100 to 240 V, 50-60 Hz | |
|--------------------|------------------------|--|
| Operating temp. | 10°C to 40°C | |
| Recommended | 20°C to 25°C | |
| Operating altitude | up to 3000 m | |
| Storage temp. | -20 °C to 60 °C | |
| Interfaces to PC | USB 2.0 (E4898A) | |
| | IEEE 1394 (ParBERT) | |
| Dimensions (W×H×D) | · · · · | |
| E4899A | 430 x 700 x 640 mm | |
| E4898A | 430 x 145 x 640 mm | |
| Bench top | 228 × 59 × 237 mm | |
| Rack mount | 19'' width | |
| | | |

Ordering Information

Agilent E4899A 100 Gb/s BERT consists of the following components:

- 1 x E4898A 100 Gb/s Front-End
- 8 x N4872A 13.5 Gb/s Generator Module
- 1 x N4873A 13.5 Gb/s Analyzer Module
- 1 x E4809A 13.5 Gb/s Central Clock Module
- 1 x E8491B Firewire Module
- 1 x E8403A VXI Mainframe
- 1 x E8257D Analog Signal Generator
- 1 x ParBERT Software
- 1 x Desktop PC
- 1 x Startup Assistance (2 days)

Accessories Included

CDs including ParBERT and 100Gb/s BERT software. RF Cables for interconnecting components and local power cords.

Related Literature

| ParBERT 81250 Product Overview | 5968-9188E |
|---|-------------|
| E8257D PSG Analog Signal Generator Data Sheet | 5989-0698EN |
| Physical Layer Test Brochure | 5988-9514EN |
| Infiniium DCA-J Wide- Bandwidth Oscilloscope Data Sheet | 5989-0278EN |

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