# Agilent N4874A ParBERT 7 Gb/s Generator
# Agilent N4875A ParBERT 7 Gb/s Analyzer

## Technical Specifications

### General

The N4874A generator and N4875A analyzer modules are each one VXI slot wide and operate in a range from 620 Mb/s up to 7 Gb/s. The ParBERT 7 Gb/s modules require the E4809A 13.5 GHz central clock module. All specifications, if not otherwise stated, are valid at the end of the recommended N4910A cable set (24" matched pair 2.4 mm).

The N4874A generator module generates hardware-based PRBS up to $2^{31}$ - 1, PRWS and user-defined patterns and provides a memory depth of 64 Mbit. The N4875A can synchronize on a 48bit detect word, or on a pure PRBS pattern without detect word.

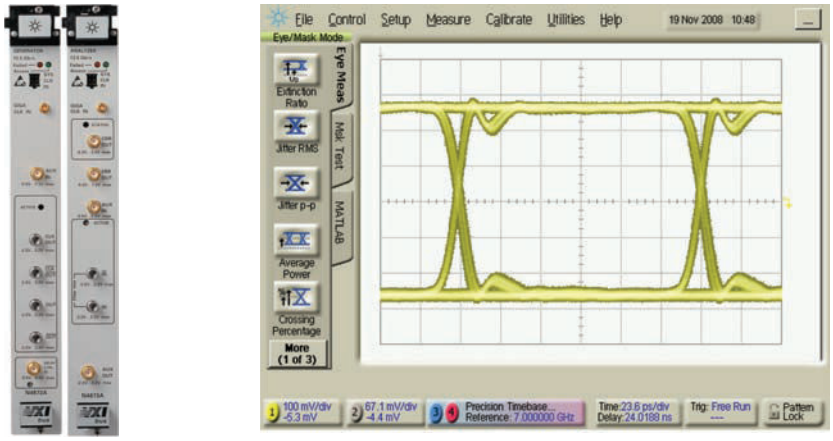


**Figure 22. N4874A & N4875A and waveform**

### Timing specifications

The ParBERT 13.5 Gb/s modules are able to work with three different clock modes.

- *Internal clock mode:*
  The common clock mode is provided by the E4809A 13.5 GHz central clock module, which generates clock frequencies up to 13.5 GHz.
- *External clock mode:*
  The system also works synchronously with an external clock, which is connected to the E4809A clock module.
- *CDR mode:*
  To use the N4875A 7 Gb/s analyzer CDR capabilities, connect the analyzer's CDR out to the E4809A clock module's clock in.

**Table 28. N4874A data generator timing specifications (@ 50% of amplitude, 50 ž to GND)**

| | |
|---|---|
| Frequency range | 620 MHz to 7 GHz |
| Delay = start delay + fine delay | Can be specified as leading edge delay in fraction of bits in each channel |
| Start delay range | 0 to 100 ns |
| Fine delay range | ± 1 period (can be changed without stopping) |
| Delay resolution | 100 fs |
| Delay accuracy | ±10 ps ± 20 ppm relative to the zero-delay placement. (@ 25 °C - 40 °C ambient temp.) |
| Relative delay accuracy | ±2 ps ± 2% typ. (@ 25 °C - 40 °C ambient temp.) |
| Skew between modules of same type | 20 ps after cable deskewing at customer levels and unchanged system frequency. (@ 25 °C - 40 °C ambient temp.) |

## Sequencing

The sequencer receives instructions from the central sequencer and generates a sequence. The channel sequencer can generate a sequence with up to 60 segments.

An analyzer channel generates feedback signals that can control the channel sequencer and/or the central sequencer. With parallel analyzer channels, the feedback is routed to the central sequencer to allow a common response of all parallel channels. With single receive channel, the channel sequencer itself handles the feedback signals.

## Pattern generation

The data stream is composed of segments. A segment can be made up of a memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 64 Mbit (at segment length resolution 512 bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to $2^{15}$ - 1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio.

A zero substitution pattern extends the longest zero series by a user selectable number of additional zeroes. The next bit following these zero series will be forced to 1. Mark ratio is the ratio of 1 s and 0 s in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4 and 7/8.

Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 512 the number of repetitions is also 512. That means that a $2^{15}$ - 1 PRBS uses up to 16 Mbit of the memory. Hardware-based PRBS can be a polynomial up to $2^{31}$ - 1. No memory is used for hardware-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. So instead of a 0 a 1 is generated and vice versa.

**Table 29. N4874A pattern and sequencing**

| **Segment length resolution** | **512 bit** |
|---|---|
| **Patterns:** | |
| **Memory based** | up to 64 Mbit |
| **PRBS/PRWS** | $2^n$ - 1, n = 7, 9, 10, 11, 15, 23, 31 |
| **Mark density** | 1/8, 1/4, 1/2, 3/4, 7/8 at $2^n$ - 1, n = 7, 9, 10, 11, 15 |
| **Errored PRBS/PRWS** | $2^n$ - 1, n = 7, 9, 10, 11, 15 |
| **Extended ones or zeros** | $2^n$ - 1, n = 7, 9, 10, 11, 15 |
| **Clock patterns** | Divide or multiply by 1, 2, 4 |
| **PRWS port width** | 1, 2 , 4, 8, 16 |

**Table 30. Data rate range, segment length resolution, available memory for synchronization and fine delay operation**

| Data rate range (Mbit/s) | Segment length resolution | Maximum memory depth (bits) |
|---|---|---|
| 620 ... 1.350,000 | 32 bits | 4,194,304 |
| 620 ... 2.700,000 | 64 bits | 8,388,608 |
| 620 ... 5.400,000 | 128 bits | 16,777.216 |
| 620 ... 7.000,000 | 256 bits | 33,554.432 |
| 620 ... 7.000,000 | 512 bits | 67,108.864 |

## N4874A generator module

The N4874A generates differential or single-ended data and clock signals operating from 620 Mb/s up to 7 Gb/s. The output levels are able to drive high-speed devices with interfaces like LVDS, ECL, PECL, CML and low voltage CMOS. The nominal output impedance is 50 Ω typical. The delay control IN has a single-ended input with 50 Ω impedance. The input voltage allows modulation of a delay element up to 1 GHz (200 ps) within the generator's differential output.

The AUX IN has a single-ended input with a 50 Ω impedance. The AUX IN allows injecting gating signals. An active (TTL high) signal at the auxiliary input forces (gates) the data to a logic zero.

## Data OUT

**Table 31. Parameters for N4874A ParBERT 7 Gb/s generator**

| | | |
|---|---|---|
| Data output | 1, differential or single ended, 2.4 mm(f) | (1) |
| Range of operation | 620 Mb/s - 7 Gb/s | |
| Impedance | 50 Ω typ. | |
| Output amplitude/resolution | 0.1 Vpp – 1.8 Vpp / 5 mV | |
| Output voltage window | –2.00 to +3.00 V | |
| Short circuit current | 72 mA max. | |
| External termination voltage | –2 V to +3 V | (2) |
| Data formats | Data: NRZ, DNRZ | |
| Addressable technologies | LVDS, CML<br>PECL - 3.3 V; ECL (terminated to 1.3 V/0 V/-2 V)<br>low voltage CMOS, LVDS, CML | |
| Transition times (20% - 80%) | < 20 ps | (3) |
| Jitter | 9 ps peak-peak typ. | (4) |
| Cross-point adjustment | 20%...80% typ. | |

(1) In single-ended mode, the unused output must be terminated with 50 Ω to GND.
(2) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
(3) At ECL levels.
(4) Clock out to data out.

## Clock OUT

**Table 32. Parameters for N4874A ParBERT 7 Gb/s generator**

| | | |
|---|---|---|
| Clock output | 1, differential or single-ended, 2.4 mm(f) | (5) |
| Frequency | 620 MHz - 7 GHz | |
| Impedance | 50 Ω typ. | |
| Output amplitude/resolution | 0.1 Vpp – 1.8 Vpp / 5 mV | |
| Output voltage window | -2.00 to +2.80 V | |
| Short circuit current | 72 mA max. | |
| External termination voltage | –2 V to +3 V | (6) |
| Addressable technologies | LVDS, CML<br>PECL; ECL (terminated to 1.3V/0 V/-2 V)<br>low voltage CMOS | |
| Transition times (10% - 90%) | < 25 ps | (7) |
| Jitter | 1 ps RMS typ. | |
| SSB phase noise (10 GHz @ 10 kHz offset, 1 Hz bandwidth) | < - 75 dBc with clock module E4809A typ. | |

(5) In single-ended mode, the unused output must be terminated with 50 Ω to GND.
(6) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
(7) At ECL levels.

## Delay control IN

**Table 33. Parameters for N4874A ParBERT 7 Gb/s generator**

| | |
|---|---|
| Delay control input | Single-ended; DC-coupled; SMA(f) |
| Input voltage window | –250 mV ... +250 mV (DC-coupled) |
| Input impedance | 50 Ω typ. |
| Delay range | –100 ps ... +100 ps |
| Modulation bandwidth | DC ... 1 GHz @ data rate < 10.5 Gb/s |

## AUX IN

**Table 34. Parameters for N4874A ParBERT 7 Gb/s generator**

| | |
|---|---|
| Interface | DC coupled, 50 Ω nominal |
| Levels | TTL levels |
| Minimum pulse width | 100 ns |
| Connector | SMA female |

## N4875A analyzer module

The analyzer features are:

- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the bit error rate

Receive memory for acquired data is up to 64 Mbit deep, depending on segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum segment resolution (32, 64, 128, 256, 512).

The analyzer is able to synchronize on a received data stream by means of a user selectable synchronization word. The sync. word has a length of 48 bits and is composed of zeros, ones and Xs ("don't cares"). The detect word must be unique within the data stream. Synchronization on a pure PRBS data-stream is done without a detect-word, instead by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ω impedance. The sensitivity of 50 mV and the common mode range of the comparator allow the testing of all common differential high-speed devices. The user has the choice of using the differential input with or without a termination voltage or as single-ended input (with a termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

**Table 35. N4875A analyzer timing: all timing parameters are measured at ECL levels, terminated with 50 Ω to GND**

| | | |
|---|---|---|
| Sampling rate | 620 MHz to 7 GHz | |
| Sample delay | Can be specified as leading edge delay in fraction of bits in each channel | |
| Start delay range | 0 to 100 ns | |
| Fine delay range | ± 1 period (can be changed without stopping) | |
| Delay resolution | 100 fs | |
| Delay accuracy | ±10 ps ± 20 ppm relative to the zero-delay placement | (1) |
| Relative delay accuracy | ±2 ps ± 2% typ. | (1) |
| Skew between modules of same type | 20 ps after cable deskewing at customer levels and unchanged system frequency. | (1) |

(1) 25 °C - 40 °C ambient temperature

**Table 36. N4875A pattern and sequencing**

| | |
|---|---|
| Analyzer auto-synchronization | On PRBS or memory-based data<br>Manual or automatic by:<br>Bit synchronization(2) with or without automatic phase alignment<br>Automatic delay alignment around a start sample delay (range: ± 10 ns)<br>BER Threshold: $10^{-4}$ to $10^{-9}$ |

(2) With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect Word at the beginning of the segment, and the generators must be on a separate system clock. Don't cares within detect word are possible. If several inputs synchronize, the delay diffference between terminals must be smaller than ±5 segment length resolution.

### Data IN

**Table 37. Parameters for N4875A ParBERT 7 Gb/s analyzer**

| | |
|---|---|
| Number of channels | 1, differential or single ended, 2.4 mm (f) |
| Range of operation | 620 Mb/s - 7 Gb/s |
| Max input amplitude | 2 Vpp |
| Input sensitivity | 50 mVpp typical @ 7 Gb/s, PRBS $2^{31}$ - 1, and BER $10^{-12}$ |
| Input voltage range | –2V ... +3 (selectable 2V window) |
| Internal termination voltage (can be switched off ) | –2.0 to +3.0 V (must be within selected 2 V window) |
| Threshold voltage range | –2.0 to + 3.0 V (must be within selected 2 V window) |
| Threshold resolution | 1 mV |
| Minimum detectable pulse width | 25 ps typ. |
| Phase margin (source: N4874A) | 1 UI - 12 ps typ. |
| Impedance | 50 Ω typ. (100 Ω differential, if termination voltage is switched off) |
| Sampling delay resolution | 100 fs |

**Table 38. Parameters for N4875A ParBERT 7 Gb/s analyzer - clock data recovery**

| | | |
|---|---|---|
| Common data rates | | |
| | S-ATA: | 1.5/3.0/6.0 Gb/s |
| | PCI-Express: | 2.5/5.0 Gb/s |
| | OC-48: | 2.488 Gbit/s |
| | 10GbE: | 3.125 Gbit/s |
| | SAN: | 3.187 Gbit/s |
| Frequency ranges | | |
| | 4.23 GHz ... 6.4 GHz | |
| | 2.115 GHz ... 3.2 GHz | |
| | 1.058 GHz....1.6 GHz | (1) |
| The CDR works with specified PRBS patterns up to $2^{31}$ - 1,<br>The CDR expects a DC balanced pattern,<br>The CDR expects an average transition density of one transition for every second bit. | | |

(1) Available for hardware S/N: DE43A00401 and software rev. 5.62

## Clock data recovery

The analyzer module has integrated CDR capabilities, which allow the recovery of either clock or data. Before the CDR can lock onto the incoming data stream, the data rate must be defined within the user interface; common data rates are pre-defined. In CDR mode, phase alignment to the center of the eye is done automatically during synchronization. For correct operation, the CDR output must be connected to the clock input of the E4809A central clock module. In addition the generator clock source and the analyzer clock source must be independent.

### AUX OUT

The AUX OUT provides data or recovered clock signals.

### AUX IN

Gating functionality: if a high level is applied at AUX IN, comparison is disabled and internal counters are stopped. After resuming a low level at AUX IN, comparison is enabled and internal counters continue. The internal sequencing is not stopped.

### ERROR OUT

Whenever one or more bit errors are detected, the error out signal is high for one segment resolution. A high period is always followed by a low period (RZ-format) in order to ensure trigger possibility on continuous errors.

**Table 39. Parameters for N4875A 7 Gb/s analyzer - AUX OUT**

| | |
|---|---|
| Interface | AC Coupled, 50 Ω nominal |
| Amplitude | 600 mV nominal |
| Output jitter (clock @ AUX OUT) | 0.01 UI rms typical |
| Connector | SMA female |

**Table 40. Upgrades 7 Gb/s - 13 Gb/s**

| Module number | Upgrade to 13.5 Gb/s |
|---|---|
| E4874A | Available on request |
| E4875A | Available on request |

**Table 41. Parameters for N4875A 13.5 Gb/s analyzer - AUX IN**

| | |
|---|---|
| Resolution | Segment resolution |
| TTL compatible | Internal 500 Ω termination to GND |
| Threshold | @ 1.5 V |
| Connector | SMA female |
| Low (0...1 V) | Internal counters are enabled |
| High (2 V...4 V) | Internal counters are stopped |
| Open | Same as low |

**Table 42. Parameters for N4875A 13.5 Gb/s analyzer - ERROR OUT**

| | |
|---|---|
| Format | RZ; active high |
| Output high level | 0 V ± 100 mV |
| Output low level | +1 V ± 100 mV |
| Connector | SMA female |

## Technical specifications

**All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10 to 40 °C ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminated with 50 Ω to ground at ECL levels if not specified otherwise.**